REMARKS

Applicant acknowledges the receipt by the Patent Office of the submission of the certified copy of the foreign priority document.

The rejection of claims 1-3, 5 and 6, under 35 USC 103(a) as being unpatentable over Booth (USP 5,543,585) in view of applicants admitted prior art is respectfully traversed.

Applicant has carefully amended claim 1 to clearly differentiate the process of the present invention from that taught in Booth. In the process of the present invention the chip/mounting area formed on the substrate includes a plurality of bond pads which are electrically connected to the substrate. A plurality of conductive elements are superimposed over the bond pads in direct alignment with the bond pads. This is controlled by screen printing the plurality of conductive elements on the bond pads. None of these steps are taught in Booth et al.

In the first step of applicants process, a plurality of conductive elements or bumps each having a flat end is formed on a chip/mounting area of the substrate by screen printing such that the conductive bumps are in direct alignment over a plurality of bond pads on the first surface of the substrate. A first encapsulant is thereafter formed to encapsulate the conductive elements or bumps wherein the flat ends of the conductive bumps are exposed and are flush with a top surface of the first encapsulant. Following this step, a chip is mounted on the first encapsulant so that the bond pads formed on the chip are electrically connected to the exposed ends of the conductive bumps. Finally, a second encapsulant is formed on the substrate to encapsulant the chip. The packaging process of the subject invention assures that no gap will be formed between the chip and the first encapsulant.

In the admitted prior art, a chip having conductive bumps thereon is mounted on a substrate in a flip-chip manner, leaving a gap (undergap) between the chip and the substrate. Then, the gap is filled by performing an underfill process. This underfill process depends on capillary action and easily causes voids to form in the filled gap known as a "popcorn effect". These drawbacks are avoided in the present invention. The admitted prior art assumes a gap will exist and that an underfill process will be used to fill it. The present invention does not require

use of the underfill process and eliminates the formation of voids otherwise associated with the underfill process.

Booth et al (USP 5,543,585) discloses two methods for preparing a substrate. Referring to Figs. 1-4, the first method is to add an insulative thermoplastic adhesive 2 to the surface of the substrate 1 and to then form holes 3 in the insulative adhesive 2 to expose conductive metal contacts 8 on the substrate 1. After the holes are formed, the holes 3 are filled with a conductive thermoplastic adhesive. This is clearly different from the process taught and claimed in the subject application. Referring to Figs. 5-7, the second method of Booth et al is to add conductive adhesive bumps 4 to the substrate 1. The bumps 4 is preferably applied by mask screening, and then the insulative adhesive 2 is applied between the bumps 4 by a selection of techniques, including print screening. Booth et al clearly makes a distinction between mask screening of the bumps 4 and screen printing of the adhesive 2. Accordingly, Booth et al does not teach or suggest screen printing a plurality of conductive elements in direct alignment over the bond pads on the first surface of the substrate much less to suggest that by doing so the underfill process is not needed. Direct alignment of the conductive elements over the bond pads also improves conduction between the substrate and the chip.

For all of the above reasons, it is clear that claim 1, as amended, is distinguishable from the teaching of Booth (USP 5,543,585) and is not obvious therefrom. Moreover, there is no basis for combining the so-called "admitted prior art" of applicant with Booth, particularly using only selected portions of the "admitted prior art" based upon hindsight, which is misleading, contrary to the teaching of the prior art and also contrary to the teaching of Booth. Accordingly, claim 1 is believed patentable over Booth and the rejection thereof should be withdrawn. Claims 2-3 and 6 are dependent claims which are believed patentable for the same reasons as given heretofore.

The rejection of claim 7 under 35 USC 103(a) as being unpatentable over Booth (USP 5,543,585) in view of applicants admitted prior art as applied to claim 1 further in view of Cook (USP 6,331,446) is respectfully traversed.

Claim 7 is a dependent claim which is believed patentable for the same reasons given heretofore in connection with claim 1. Moreover, the Examiner allegedly states that it is

obvious to combine a second encapsulant to form a fillet around the edges of the chip without encapsulating the outer surface of the chip in accordance with the teaching of Booth et al and applicants admitted prior art. This is contrary to the teaching of Booth et al and the admitted prior art.

The use of an underfill process is clearly disclosed in Cook et al and the underfill material (26) is used to enclose and seal the other underfill material (24). As stated in Cook et al in Col. 1, lines 60-62, the release of moisture during the underfill process may create voids in the underfill material and the bumps may extrude into the voids during thermal loading particularly for packages with a relatively high bump density (Col. 2, lines 3-5). Some of the same problems are identified by Applicant in the admitted prior art and are associated with the underfill process. Cook et al makes reference to the void formations associated with the underfill process which Cook et al considers necessary. This is contrary to the teachings of the present invention which is to avoid using the underfill process so as to entirely prevent the formation of voids between the chip and the substrate. Accordingly, applicant does not understand how the Examiner could be using the combination of applicants admitted prior art and the teaching of Cook et al as explained above, to render claim 7 obvious without merely selecting features of each based on the teaching of Applicant.

For all of the above reasons, claim 7 is clearly patentable over the combination of Booth '585 in view of applicants admitted prior art and Cook '446.

The rejection of claim 8 under 35 USC 103(a) as being unpatentable over Booth '585 in view of applicants admitted prior art, further in view of Lai (USP 6,323,066) is respectfully traversed. There is no teaching in Booth or in the admitted prior art or in Lai et al of screen printing a plurality of conductive elements over the pads in direct alignment with the pads. This feature is significant to the present invention eliminating the need for using an underfill process. Accordingly, the rejection of claim 8 which is a dependent claim, should be withdrawn.

Reconsideration and allowance of claims 1-3, and 5-8 is respectfully solicited.

Respectfully submitted,

Eugene Lieberstein
Reg. No. 24,645

ANDERSON, KILL & OLICK
1251 Avenue of the Americas
New York, New York 10020-1182

MAILING CERTIFICATE

I hereby certify that this correspondence is being deposited with the U.S. Postal Service as first class mail in an envelope addressed: Commissioner of Patents & Trademarks, Washington, DC 20231 on October 2, 2003.

Date: October 2, 2003

1. (Currently Amended) A packaging process for a semiconductor package, comprising the steps of:

1) preparing a substrate having a first surface and a second surface, wherein at least one chip-mounting area is formed on the first surface with the first surface having a first plurality of bond pads electrically connected to the substrate;

2) ~~disposing~~ screen printing a plurality of conductive elements on the chip-mounting area of the substrate in direct alignment over each of said first plurality of bond pads, wherein the conductive elements are electrically connected to the substrate and each formed with a flat end;

3) forming a first encapsulant by a printing process on the chip-mounting area of the substrate for encapsulating the conductive elements, wherein the first encapsulant formed by printing is adapted to have a top surface thereof formed in coplanar alignment with the flat ends of the conductive elements to thereby form a common coplanar surface, and the ends of the conductive elements are exposed to the outside of the first encapsulant;

4) preparing at least one semiconductor chip having a second plurality of bond pads formed on a surface thereof, and mounting the semiconductor chip on the top surface of the first encapsulant in a manner that the second bond pads are electrically connected to the exposed ends of the conductive elements respectively and with the surface of the semiconductor chip closely attached to the coplanar surface formed by the first encapsulant and conductive elements free of any gap between the semiconductor chip and the coplanar surface;

5) forming a second encapsulant on the first surface of the substrate for encapsulating the chip; and

6) implanting a plurality of solder balls on the second surface of the substrate, wherein the solder balls are electrically connected to the substrate.

2. (Original) The packaging process of claim 1, wherein the conductive elements are conductive bumps.

3. (Original) The packaging process of claim 2, wherein the conductive bumps are made of tin, lead or tin/lead alloy.

4. (Cancelled)

5. (Cancelled)

6. (Original) The packaging process of claim 1, wherein the chip has a surface with no bond pads formed thereon encapsulated by the second encapsulant.

7. (Original) The packaging process of claim 1, wherein the chip has a surface with no bond pads formed thereon exposed to the outside of the second encapsulant for directly contacting the atmosphere.

8. (Previously Amended) The packaging process of claim 1, further comprising a step of attaching a heat sink to the first surface of the substrate after the step (4) of mounting the chip on the first encapsulant, allowing the heat sink to be encapsulated by the second encapsulant in the step (5) of forming the second encapsulant.